ABSTRACT

A system and method for generating multiple drive strengths for one or more output signals of a memory controller operable to control a memory subsystem. The system includes a state machine operable to generate an n-bit output representative of a drive strength operable to drive the one or more output signals; and a plurality of adders, each adder having a plurality of n-bit inputs, each input receiving a selective set of bits from the n-bit output of the state machine, the adders generating a plurality of n-bit outputs representative of drive strengths operable to drive the output signals. The method includes generating an n-bit output representative of a drive strength, and adding combinations of two or more selective sets of bits from the n-bit output to generate a plurality of n-bit outputs representative of a plurality of drive strengths that are operable to drive the output signal.

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